Information Disclosure Statement By Applicant

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Filing Date: **04/19/2004**
First Named Inventor: **King**
Art Unit: **2811**
Examiner Name: **N/A**
Attorney Docket Number: **PRG2001-5CD3**

Examiner Initials	Patent Number	Publication Date	Inventor Name
DM	US 3,558,736	06-28-1971	McGroddy
DM	US 3,651,426	03-21-1972	Boatner et al.
DM	US 3,974,486	08-10-1976	Curtis et al.
DM	US 4,047,974	09-13-1977	Harari
DM	US 4,143,393	03-06-1979	DiMaria et al.
DM	US 4,686,550	08-11-1987	Capasso et al.
DM	US 4,806,998	02-21-1989	Vinter et al.
DM	US 4,851,886	07-25-1989	Lee et al.
DM	US 4,903,092	02-20-1990	Luryi et al.
DM	US 4,945,393	07-31-1990	Beltram et. al.
DM	US 5,021,841	06-04-1991	Leburton et al.
DM	US 5,023,836	06-11-1991	Mori
DM	US 5,032,877	07-16-1991	Bate
DM	US 5,032,891	07-16-1991	Takagi et al.
DM	US 5,055,891	10-08-1991	Moll et al.
DM	US 5,084,743	01-28-1992	Mishra et al.
DM	US 5,093,699	03-03-1992	Weichold et al.
DM	US 5,130,763	07-14-1992	Delhaye et al.
DM	US 5,162,880	11-10-1992	Hazama
DM	US 5,189,499	02-23-1993	Izumi et al.
DM	US 5,250,815	10-05-1993	Battersby et al.
DM	US 5,258,624	11-02-1993	Battersby et al.
DM	US 5,302,838	04-12-1994	Roenker et al.
DM	US 5,357,134	10-18-1994	Shimoji
DM	US 5,390,145	02-14-1995	Nakasha et al.
DM	US 5,442,194	08-15-1995	Moise
DM	US 5,448,513	09-05-1995	Hu et al.
DM	US 5,455,432	10-03-1995	Hartsell et al.
DM	US 5,463,234	10-31-1995	Toriumi et al.
DM	US 5,477,169	12-19-1995	Shen et at.
DM	US 5,523,603	06-04-1996	Fishbein et al.
DM	US 5,543,652	08-06-1996	Ikeda et al.
DM	US 5,606,177	02-25-1997	Wallace et al.
DM	US 5,633,178	05-27-1997	Kalnitsky
DM	US 5,675,157	10-07-1997	Battersby
DM	US 5,689,458	11-18-1997	Kuriyama
DM	US 5,698,997	12-16-1997	Williamson III et al.

Examiner Signature: [signature] **Date Considered:** 4/26/05

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Examiner Initials	Patent Number	Publication Date	Inventor Name
DM	US 5,705,827	01-06-1998	Baba et al.
DM	US 5,732,014	03-24-1998	Forbes
DM	US 5,742,092	04-21-1998	Zotov et al.
DM	US 5,761,114	06-02-1998	Bertin et al.
DM	US 5,770,958	06-23-1998	Arai et al.
DM	US 5,773,996	06-30-1998	Takao
DM	US 5,798,965	08-25-1998	Jun
DM	US 5,804,475	09-08-1998	Meyer et al.
DM	US 5,843,812	12-01-1998	Hwang
DM	US 5,869,845	02-09-1999	Van der Wagt et al.
DM	US 5,883,549	03-16-1999	De Los Santos
DM	US 5,883,829	03-16-1999	Van der Wagt
DM	US 5,895,934	04-20-1999	Harvey et al.
DM	US 5,903,170	05-11-1999	Kulkarni et al.
DM	US 5,907,159	05-25-1999	Roh et al.
DM	US 5,936,265	08-10-1999	Koga
DM	US 5,945,706	08-31-1999	Jun
DM	US 5,953,249	09-14-1999	Van der Wagt
DM	US 5,959,328	09-28-1999	Krautschneider et al.
DM	US 5,962,864	10-05-1999	Leadbeater et al.
DM	US 6,015,739	01-18-2000	Gardner et al.
DM	US 6,015,978	01-18-2000	Yuki et al.
DM	US 6,075,265	06-13-2000	Goebel et al.
DM	US 6,077,760	06-20-2000	Fang et al.
DM	US 6,084,769	07-04-2000	Kozicki et al.
DM	US 6,091,077	07-18-2000	Morita et al.
DM	US 6,097,036	08-01-2000	Teshima et al.
DM	US 6,104,631	08-15-2000	El-Sharawy et al.
DM	US 6,128,216	10-03-2000	Noble Jr. et al.
DM	US 6,130,559	10-03-2000	Balsara et al.
DM	US 6,150,242	11-21-2000	Van der Wagt et al.
DM	US 6,184,539	02-06-2001	Wu et al.
DM	US 6,194,303	02-27-2001	Alphenaar et al.
DM	US 6,205,054	03-20-2001	Inami
DM	US 6,222,766	04-24-2001	Sasaki et al.
DM	US 6,225,165	05-01-2001	Noble Jr. et al.
DM	US 6,246,606	06-12-2001	Forbes et al.

Examiner Signature: [signature] **Date Considered:** 4/26/05

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Examiner Initials	Patent Number	Publication Date	Inventor Name
DM	US 6,261,896	07-17-2001	Jun
DM	US 6,294,412	09-25-2001	Krivokapic
DM	US 6,301,147	10-09-2001	El-Sharawy et al.
DM	US 6,303,942	10-16-2001	Farmer
DM	US 6,310,799	10-30-2001	Duane et al.
DM	US 6,396,731	05-28-2002	Chou
DM	US 6,404,018	06-11-2002	Wu et al.
	Publication Number	**Publication Date**	**Inventor Name**
DM	US 2001/0005327 A1	06-28-2001	Duane et al.
DM	US 2001/0013621 A1	08-16-2001	Nakazato
DM	US 2001/0019137 A1	09-06-2001	Koga et al.
DM	US 2001/0024841 A1	09-27-2001	Noble Jr. et al.
DM	US 2001/0053568 A1	12-20-2001	Deboy et al.
DM	US 2002/0093030 A1	07-18-2002	Hsu et al.
DM	US 2002/0100918 A1	08-01-2002	Hsu et al.
DM	US 2002/0109150 A1	08-15-2002	Kajiyama

Examiner Initials	Foreign Publications	Publication Date	Name of Patentee or Applicant of Cited Patent
DM	EP 0747940 A2	12-11-1996	SGS-Thomsom
DM	EP 0747961 A2	12-11-1996	SGS-Thomsom
DM	EP 0655788 B1	01-21-1998	SGS-Thomsom
DM	EP 1050964 A2	11-08-2000	NEC Corporation
DM	EP 1085656 A2	03-21-2001	Texas Instruments
DM	EP 1107317 A1	06-13-2001	Hitachi
DM	EP 0526897 B1	11-07-2001	NEC
DM	EP 1168456 A2	01-02-2002	Progressant Technologies
DM	EP 1204146 A1	05-08-2002	Hitachi Ltd.
DM	WO 90/03646	04-05-1990	Dallas Semiconductor Corp.
DM	WO 99/63598	04-20-1999	Stanford
DM	WO 00/41309	07-13-2000	Raytheon Company
DM	WO 01/65597 A1	09-07-2001	Motorola, Inc.
DM	WO 01/69607 A2	09-20-2001	Motorola, Inc.
DM	WO 01/99153 A2	12-27-2001	Progressant Technologies

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Examiner Initials	Other Publications
DM	Final Report: SMILE MEL-ARI Project n°28741 – Chapter V, pp. 184-194.
DM	News Release from www.eurekalert.org/releases/udel-udcnflb.html, " UD Computer News: Future Looks Bright for Tunnel Diodes, Promising Faster, More Efficient Circuits," October 1, 1998, 4 pages.
DM	P. S. BARLOW, et al., "Negative differential output conductance of self-heated power MOSFETs," IEE Proceedings-I Solid-State and Electron Devices, Vol 133, Part I, No. 5, October 1986, pp. 177-179.
DM	E. CHAN, et al., "Compact Multiple-Valued Multiplexers Using Negative Differential Resistance Devices," IEEE Journal of Solid-State Circuits, Vol. 31, No. 8, August 1996, pp. 1151-1156.
DM	E. CHAN, et al., "Mask Programmable Multi-Valued Logic Gate Arrays Using RTDs and HBTs," IEE Proceedings-E: Computers and Digital Techniques, Vol. 143, No. 5, October 1996, pp. 289-294.
DM	Deen, Jamal (editor) et al., excerpt from "CMOS RF modeling, characterization and applications," World Scientific, April 2002, 34 pages.
DM	DOZSA, L. et al., "A transient method for measuring current-voltage characteristics with negative differential resistance regions," Research Institute for Technical Physics, P. O. Box 76, H-1325 Budapest, Hungary, (Received July 24, 1997; accepted August 1, 1997), 2 pages.
DM	GARDNER, CARL, RINGHOFER, CHRISTIAN, "Smooth Quantum Hydrodynamic Model Simulation of the Resonant Tunneling Diode," Dept. Of Mathematics Arizona State University, pp. 1-5, (1998).
DM	GEPPERT, Linda, "Quantum transistors: toward nanoelectronics," IEEE Spectrum, September 2000, pp. 46-51.
DM	GOLDHABER-GORDON, David et al., "Overview of nanoelectronic devices," Proc. IEEE, 85(4), April 1997, pp. 521-540.
DM	ALEJANDRO F. GONZALEZ, et al., "Standard CMOS Implementation of a Multiple-Valued Logic Signed-Digit Adder Based on Negative Differential-Resistance Devices," Proceedings of the 30th IEEE International Symposium on Multiple-Valued Logic (ISMVL 2000), 6 pages.
DM	HADDAB, Y. et al., "Quantized current jumps in silicon photoconductors at room temperature," J. Appl. Phys. 86 (7), 1 October 1999, pp. 3787-3791.
DM	G. I. HADDAD et al., "Tunneling Devices and Applications in High Functionality/Speed Digital Circuits," Solid State Electronics, Vol. 41, No. 10, Oct. 1997, pp. 1515-1524.
DM	HANSCH, W. et al., "The planar-doped-barrier-FET: MOSFET overcomes conventional limitations," ESSDERC'97 27th European Solid-State Device Research Conference, Stuttgart, 22-24 September 1997, 4 pages.
DM	C. P. HEIJ, et al., "Negative Differential Resistance Due to Single-Electron Switching," Applied Physics Letters, Vol. 74, Number 7, February 15, 1999, 5 pages.
DM	HONG, J.W. et al, "Local charge trapping and detection of trapped charge by scanning capacitance microscope in SiO2/Si system," Appl. Phys. Lett., 75 (12), Sept. 20, 1999, pp. 1760-1762.
DM	JUNGEL, A, POHL, C., "Numerical Simulation of Semiconductor Devices: Energy-Transport and Quantum Hydrodynamic Modeling," Fachbereich Math., Tech. Univ. Berlin, Germany, pp.1-9, 1998.
DM	KARNA, Shashi P. et al., "Point defects in SI-SIO2 systems: current understanding," Published in G. Pacchioni et al. (eds.), "Defects in SIO2 and related dielectrics: science and technology," Kluwer Academic Publishers, p. 599-615, (2000), 19 pages.

Examiner Signature: [signature]

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Examiner Initials	Other Publications
DM	KING, Tsu-Jae et al., Serial number 09/602,658, entitled "CMOS Compatible Process for Making a Tunable Negative Differential Resistance (NDR) Device," filed June 22, 2000, 33 pages.
DM	KING, Tsu-Jae et al., Serial number 09/603,101, entitled "CMOS-Process Compatible, Tunable NDR (Negative Differential Resistance) Device and Method of Operating Same," filed June 22, 2000, 34 pages.
DM	KING, Tsu-Jae et al., Serial number 09/603,102, entitled "Charge Trapping Device and Method for Implementing a Transistor having a Negative Differential Resistance Mode," filed June 22, 2000, 39 pages.
DM	S. J. KOESTER, et al., "Negative Differential Conductance in Lateral Double-Barrier Transistors Fabricated in Strained Si Quantum Wells," Applied Physics Letters, Vol. 70, No. 18, May, 1997, pp. 2422-2424.
DM	O. LE NEEL, et al., "Electrical Transient Study of Negative Resistance in SOI MOS Transistors," Electronics Letters, Vol 26, No 1, pp. 73-74, Jan 1990.
DM	S. LURYI and M. MASTRAPASQUA, "Light-emitting Logic Devices based on Real Space Transfer in Complementary InGaAs/InAlAs Heterostructures", in "Negative Differential Resistance and Instabilities in 2D Semiconductors", ed. by N. Balkan, B. K. Ridley, and A. J. Vickers, NATO ASI Series [Physics] B 307, pp. 53-82, Plenum Press (New York 1993).
DM	SERGE LURYI and MARK PINTO, "Collector-Controlled States and the Formation of Hot Electron Domains in Real-Space Transfer Transistors," AT&T Bell Laboratories, pp. 1-7, 1992.
DM	SERGE LURYI and MARK PINTO, "Collector-Controlled States in Charge Injection Transistors," SPIE-92 Symposium, pp. 1-12, 1992.
DM	R. H. MATHEWS, et al., "A New RTD-FET Logic Family," Proceedings of the IEEE, Vol. 87, No. 4, pp. 596-605, 1999.
DM	P. MAZUMDER, et al., "Digital Circuit Applications of Resonant Tunneling Devices," Proceedings of the IEEE, Vol. 86, No. 4, pp. 664-686, April, 1998.
DM	S. MOHAN, et al., "Logic Design Based on Negative Differential Resistance Characteristics of Quantum Electronic Devices," IEE Proceedings-G: Electronic Devices, Vol. 140, No. 6, Dec. 1993, pp. 383-391.
DM	S. MOHAN, et al., "Ultrafast Pipelined Adders Using Resonant Tunneling Transistors," IEE Electronics Letters, Vol. 27, No. 10, May 1991, pp. 830-831.
DM	S. MOHAN, et al., "Ultrafast Pipelined Arithmetic Using Quantum Electronic Devices," IEE Proceedings-E: Computers and Digital Techniques, Vol. 141, No. 2, Mar. 1994, pp. 104-110.
DM	FARID NEMATI et al., "A Novel High Density, Low Voltage SRAM Cell With a Vertical NDR Device," Center for Integrated Systems, Stanford University, CA, (2 pages).
DM	FARID NEMATI et al., "A Novel Thyristor-based SRAM Cell (T-RAM) for High-Speed, Low-Voltage, Giga-scale Memories," Center for Integrated Systems, Stanford University, CA, (4 pages).
DM	S.M.A. NIMOUR, R. OUASTI, N. ZEKRI, "Effect of Spatially Disordered Barriers on the Band Structure of Finite Superlattices," phys. stat. sol. (b) 1998, 209, No. 2, 311-318.
DM	R. OBERHUBER, et al., "Tunnel-Devices with Negative Differential Resistivity Based on Silicon?," Source: Deutsche Forschungsgemeinschaft and Siemens AG, date unknown, 2 pages.
DM	C. PACHA, et al., "Resonant Tunneling Device Logic Circuits," Microelectronics Advanced Research Initiative (MEL-ARI,) July 1998-July 1999, pp. 1-22.

Examiner Signature: [signature]

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Examiner Initials	Other Publications
DM	C. PACHA and K. GOSER, "Design of Arithmetic Circuits using Resonant Tunneling Diodes and Threshold Logic," Lehrstuhl Bauelemente der Elektrotechnik, Universitat Dortmund, pp. 1-11, September 1997.
DM	S. L. ROMMEL, et al., "Room Temperature Operation of Epitaxially Grown Si/Si0.5Ge0.5/Si Resonant Interband Tunneling Diodes," Applied Physics Letters, Vol. 73, No. 15, pp. 2191-2193, 1998.
DM	SCOFFIELD, John H. et al., "Reconciliation of different gate-voltage dependencies of 1/f noise in n-MOS and p-MOS transistors," IEEE Trans. Electron. Dev. 41 (11), 11 pgs.
DM	A. SEABAUGH, "Promise of Tunnel Diode Integrated Circuits," Tunnel Diode and CMOS/HBT Integration Workshop, December 9, 1999, Naval Research Laboratory, Washington, DC., 13 Pages.
DM	SEABAUGH A., BRAR B., BROEKAERT T., MORRIS F., and FRAZIER G., "Resonant Tunneling Mixed Signal Circuit Technology," Solid-State Electronics 43:1355-1365, 1999.
DM	SEABAUGH, A. et al., "Tunnel-Diode IC," Minneapolis, October 2, 2001, 23 pages.
DM	SHAO, Z., POROD, W., LENT, C., & KIRKNER, D., "Transmission Zero Engineering in Lateral Double-Barrier Resonant Tunneling Devices," Dept. Of Electrical Engineering, University of Notre Dame, pp. 1-7 (1996).
DM	SHOUCAIR F. et al., "Analysis and Simulation of Simple Transistor Structures Exhibiting Negative Differential Resistance," EECS Department, UC Berkeley, Berkeley CA, (4 pages).
DM	J. P. SUN, et al., "Resonant Tunneling Diodes: Models and Properties," Proceedings of the IEEE, Vol. 86, No. 4, April 1998, pp. 641-661.
DM	J. P. A. VAN DER WAGT, "Tunneling-Based SRAM," Proceedings of the IEEE, Vol. 87, No. 4, pp. 571-595, 1999.
DM	J. P. A. VAN DER WAGT, et al., "RTD/HFET Low Standby Power SRAM Gain Cell," Source: Corporate Research Laboratories, Texas Instruments, 1998, 4 pages.
DM	VILLA, S. et al., "Application of 1/f noise measurements to the characterization of near-interface oxide states in ULSI n-MOSFET's," Dipartimento di Elettronica e nformazione, Politecnico di Milano (Italy), 7 pages.
DM	WIRTH, G. et al., "Periodic transconductance oscillations in sub-100nm MOSFETs," ESSDERC'97 27th European Solid-State Device Research Conference, Stuttgart, 22-24 September 1997, 4 pages.
DM	G. WIRTH, et al., "Negative Differential Resistance in Ultrashort Bulk MOSFETs," IECON'99 Conference Proceedings, Vol. 1, San Jose, 1999, S. 29 - 34.
DM	JIAN FU ZHANG, "Traps: Detrapping," Wiley Encyclopedia of Electrical and Electronics Engineering Online, Article Posting Date: December 27, 1999, John Wiley & Sons, Inc., 4 Pages.
DM	JIAN FU ZHANG, "Traps: Effects of Traps and Trapped Charges on Device Performance," Wiley Encyclopedia of Electrical and Electronics Engineering Online, Article Posting Date: December 27, 1999, John Wiley & Sons, Inc., 2 Pages.
DM	JIAN FU ZHANG, "Traps: Measurement Techniques," Wiley Encyclopedia of Electrical and Electronics Engineering Online, Article Posting Date: December 27, 1999, John Wiley & Sons, Inc., 5 Pages.
DM	JIAN FU ZHANG, "Traps: Origin of Traps," Wiley Encyclopedia of Electrical and Electronics Engineering Online, Article Posting Date: December 27, 1999, John Wiley & Sons, Inc., 4 pages.
DM	JIAN FU ZHANG, "Traps: Trapping Kinetics," Wiley Encyclopedia of Electrical and Electronics Engineering Online, Article Posting Date: December 27, 1999, John Wiley & Sons, Inc., 2 Pages.

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Examiner Initials	Other Publications
DM	JIAN FU ZHANG, "Traps," Wiley Encyclopedia of Electrical and Electronics Engineering Online, Article Posting Date: December 27, 1999, John Wiley & Sons, Inc., 2 Pages.
DM	ZHANG, J.F. et al., "A comparative study of the electron trapping and thermal detrapping in SiO2 prepared by plasma and thermal oxidation," J. Appl. Phys. 72 (4), 15 August 1992, pp. 1429-1435.
DM	ZHANG, J.F. et al., "A quantitative investigation of electron detrapping in SiO2 under Fowler-Nordheim stress," J. Appl. Phys. 71 (12), 15 June 1992, pp. 5989-5996.
DM	ZHANG, J.F. et al., "Electron trap generation in thermally grown SiO2 under Fowler-Nordheim stress," J. Appl. Phys. 71 (2), 15 January 1992, pp. 725-734.

Examiner Signature: 

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